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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/475,452 12/30/99 MURTHY

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MICHAEL A BERNADICOU
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES CA 90025

EXAMINER

LEE, E

ART UNIT	PAPER NUMBER
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2815

DATE MAILED:

08/09/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/475,452	Applicant(s) MURTHY ET AL.
	Examiner Eugene Lee	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 December 1999.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) 16-18 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-15 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 December 1999 is/are objected to by the Examiner.
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) Notice of References Cited (PTO-892) 18) Interview Summary (PTO-413) Paper No(s). _____ .
- 16) Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) Notice of Informal Patent Application (PTO-152)
- 17) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 20) Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-15) in Paper No. 6 is acknowledged.
2. Claims 16-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Election was made without traverse in Paper No. 5.

Drawings

3. FIG. 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).
4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "302" has been used to designate both n-well and p-well. See, for example, page 13, line 11 and page 13, line 27. Correction is required.
5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: element 324. See, for example, page 19, line 15. Correction is required.

Specification

6. The disclosure is objected to because of the following informalities: on page 9, line 16, the word "then" should be "than." This typographical error also appears in other sections of the specification and all instances should be corrected.

Claim Objections

7. Claim 4 is objected to because of the following informalities: the word “then” should be “than.” Appropriate correction is required.
8. Claim 10 is objected to because of the following informalities: the “method” should be “product” based on its dependency to claim 1. Appropriate correction is required.

Claim Rejections - 35 USC §102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

10. Claims 1, 8, 9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Krivokapic ‘587. Krivokapic discloses (see, for example, FIG. 2p) a transistor (MOS device) 300 comprising a substrate (first conductivity region) 201, gate oxide (gate dielectric) 208, gate (gate electrode) 210, spacer (sidewall spacers) 219, source 217 and drain 218. The distance between the source and drain define a channel where the distance directly beneath the gate electrode is larger than the distance deeper into the substrate. Regarding claim 12, see, for example, column 9, lines 19-40 and element 241.

11. Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Takeuchi ‘351. Takeuchi discloses (see, for example, FIG. 11c) a MOSFET comprising a gate insulator (gate

dielectric) 3, gate electrode 4, thin insulator (sidewall spacer) 6B, and source/drain junction surface (silicon or silicon alloy regions) 9B.

12. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Choi '582. See, for example, FIG. 2.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 in view of Takeuchi '351. Krivokapic does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric.

However, Takeuchi teaches (see, for example, FIG. 11(c)) a MOSFET comprising elevated source and drain regions 7B comprising a facet. In column 12, lines 45-63, Takeuchi teaches that such a structure provides reduced parasitic capacitance. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use this structure in Krivokapic's invention in order to reduce parasitic capacitance.

15. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 as applied to claim 1 above, and further in view of Choi '582. Krivokapic does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate

dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film of Choi in Krivokapic's invention in order to reduce hot carrier effects.

16. —— Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi '582. Krivokapic in view of Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film of Choi in Krivokapic in view of Takeuchi in order to reduce hot carrier effects.

17. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587 in view of Choi et al. '088. Krivokapic does not disclose a pair of deposited silicon or silicon alloy regions having a first conductivity type formed between said pair of deposited silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region. However, Choi (see, for example, FIG. 2 and FIG. 3) a structure 106 comprising halo regions 120, 122. Choi teaches that halo regions provide higher

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punchthrough voltage. Therefore, it would have been obvious to use halo regions in Krivokapic's device in order to attain a higher punchthrough voltage.

18. Claims 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic '587. Krivokapic does not disclose an inflection point which occurs of between 50-200A laterally beneath said gate electrode and at a depth of between 25-200A beneath said gate dielectric. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these depths, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 10 and 11, Krivokapic does not disclose the concentration of said deposited silicon or silicon alloy source/drain regions of a second conductivity type having a concentration between $1 \times 10^{18} / \text{cm}^3 - 3 \times 10^{21} / \text{cm}^3$ or approximately $1 \times 10^{21} / \text{cm}^3$. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these concentrations, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi '351 in view of Choi '582. Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edges of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the gate insulating film of Choi in Takeuchi's invention in order to reduce hot carrier effects.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
August 4, 2001



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800